Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A method for producing a circuit board having an integrated electronic component comprising:

providing a circuit board substrate having a first substrate surface and a second substrate surface;

securing a first integrated electronic component to the first substrate surface;

disposing a first dielectric layer on the first substrate surface and over the first integrated electronic component;

disposing a metallic layer on the first dielectric layer to produce an integrated electronic component assembly;

producing in the integrated electronic component assembly at least one via having a metal lining in contact with said metallic layer;

disposing a second dielectric layer over said via and over said metallic layer;

producing at least one opening in the second dielectric layer and in the first dielectric layer to expose at least part of the first integrated electronic component; and

forming a metal lining in said opening and coupled to the first integrated electronic component to produce a circuit board having at least one integrated electronic component.

Claim 2 (withdrawn): The method of Claim 1 wherein said circuit board substrate includes a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface;

Claim 3 (withdrawn): The method of Claim 1 wherein said circuit board substrate comprises a multi-layer core substrate.

Claim 4 (withdrawn): The method of Claim 2 wherein said circuit board substrate comprises a multi-layer core substrate.

Claim 5 (withdrawn): The method of Claim 1 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

Claim 6 (withdrawn): The method of Claim 2 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

Claim 7 (withdrawn): The method of Claim 3 wherein said circuit board substrate includes said at least one via passing through said circuit board from said first substrate surface to said second substrate surface.

Claim 8 (withdrawn): The method of Claim 2 additionally comprising patterning said first metallic layer to expose at least a portion of said first substrate surface, said first integrated electronic component being secured to said portion of said first substrate surface.

Claim 9 (withdrawn): The method of Claim 8 additionally comprising patterning said second metallic layer to expose at least a portion of said second substrate surface.

Claim 10 (withdrawn): The method of Claim 9 additionally comprising connecting a second integrated electronic component to said portion of said second substrate surface.

Claim 11 (withdrawn): The method of Claim 9 additionally comprising forming a cavity in said portion of said second substrate surface, and disposing a second integrated electronic component in said cavity.

Claim 12 (withdrawn): The method of Claim 1 wherein said first integrated electronic component includes at least one first pad in contact with said metal lining in said opening.

Claim 13 (withdrawn): The method of Claim 1 additionally comprising producing in the integrated electronic component assembly at least one blind via through said metallic layer and through said first dielectric layer, said blind via being lined with a metal via which is coupled to said metallic layer.

Claim 14 (withdrawn): The method of Claim 1 wherein said via extends entirely through the integrated electronic component assembly.

Claim 15 (withdrawn): The method of Claim 13 wherein said via extends entirely through the integrated electronic component assembly.

Claim 16 (withdrawn): The method of Claim 8 additionally comprising disposing a patterned metallic layer over the second dielectric layer.

Claim 17 (currently amended): A multi-layer printed circuit board having at least one integrated electronic component comprising:

a circuit board substrate comprising the core of said multi-layer printed circuit board and having a first substrate surface and a second substrate surface;

a first integrated electronic component, ~~secured to the first substrate surface;~~ where said first integrated electronic component is a prefabricated component;

an adhesive securing said first integrated electronic component and said first substrate;

a first dielectric layer disposed on ~~the~~ said first substrate surface and over ~~the~~ said first integrated electronic component;

a metallic layer disposed on ~~the~~ said first dielectric layer;

at least one via passing through ~~the~~ said first dielectric layer and having a metal lining in contact with said metallic layer; and

a second dielectric layer disposed over said via and over said metallic layer,

said first dielectric layer and said second dielectric layer having a structure defining at least one opening exposing at least part of ~~the~~ said first integrated electronic component, said opening supporting an opening metal lining which is coupled to ~~the~~ said first integrated electronic component.

Claim 18 (currently amended): The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on ~~the~~ said first substrate surface and a second metallic layer disposed on said second substrate surface.

Claim 19 (original): The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate.

Claim 20 (original): The multilayer printed circuit board of Claim 17 wherein said at least one via passes from said first substrate surface to said second substrate surface.

Claim 21 (original): The multilayer printed circuit board of Claim 18 wherein said at least one via passes from said first substrate surface to said second substrate surface.

Claim 22 (original): The multilayer printed circuit board of Claim 18 wherein said first metallic layer comprises a patterned first metallic layer to expose at least a portion of said first substrate surface, said first integrated electronic component being secured to said exposed portion of said first substrate surface.

Claim 23 (original): The multilayer printed circuit board of Claim 18 wherein said second metallic layer comprises a patterned second metallic layer to expose at least a portion of said second substrate surface.

Claim 24 (original): The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

Claim 25 (original): The multilayer printed circuit board of Claim 23 wherein said exposed portion of said second substrate surface includes a cavity.

Claim 26 (original): The multilayer printed circuit board of Claim 25 additionally comprising a second integrated electronic component disposed in said cavity.

Claim 27 (original): The multilayer printed circuit board of Claim 17 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 28 (original): The multilayer printed circuit board of Claim 25 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 29 (original): The multilayer printed circuit board of Claim 26 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 30 (original): The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 31 (original): The multilayer printed circuit board of Claim 25 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 32 (original): The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 33 (original): The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 34 (original): The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

Claim 35 (withdrawn) A method for producing a circuit board having an integrated electronic component comprising:

providing a circuit board substrate having a first substrate surface and a second substrate surface;

securing a first integrated electronic component to the first substrate surface;

disposing a first dielectric layer on the first substrate surface and over the first integrated electronic component;

producing at least one via;

disposing a metallic layer on the first dielectric layer and in the via to produce an integrated electronic component assembly;

disposing a second dielectric layer over said metallic layer;

producing at least one opening in the second dielectric layer and in the first dielectric layer to expose at least part of the first integrated electronic component; and

forming a metal lining in said opening and coupled to the first integrated electronic component to produce a circuit board having at least one integrated electronic component.